REMARKS

The Examiner's attention is directed to the Information Disclosure Statement filed by certificate on February 5, 2002, and to the Submittal of Priority Documents filed by certificate on March 20, 2002.

In the Office Action, the Examiner rejected claims noted that the certified priority documents had not been filed, rejected claims 1 - 6, and 8 - 10 as anticipated by Bailey et al., rejected claims 7, 11 and 12 as obvious over Bailey and UK 2,326,023, and rejected claims 13 and 14 as obvious over Bailey.

Priority Documents

As noted above, the priority documents have been forwarded to the Examiner. Acknowledgment thereof is hereby requested.

35 U.S.C. §102(b)

The Bailey et al. reference provides an array of LEDs in an x-y matrix. The LEDs are individually addressed by, for example, a raster-scanning address circuit to display a video signal. Each of the light-emitting diodes are connected to a corresponding memory circuit element via flip-flops. The array is a sandwich structure comprising a monolithic array 43 of individual light-emitting diodes 43a, 43b and so forth and a monolithic silicon large scale integrated circuit (LSI) 44 with a multilayer metallization and spherical interconnections generally indicated at 45 sandwiched between the two. The LSI silicon circuit comprising the array of memory elements is mounted on a metallic heat sink 46. The light is generated at the p-n junctions back of the crystal of the array 43, or adjacent the interconnections 45 with the

LSI circuit 44. The monolithic array of light-emitting devices 43 is shown deeply etched on the p-n junction side at 48 providing deep channels which form a grid which isolates each light-emitting diode area. Such an etched grid has two advantages. First, it provides a reflector system to improve light from the array 43. Second, the grid effectively reduces the optical cross-talk between adjacent elements in the array because of the optical isolation it provides. The channels of the grid 48 effectively cause the back surface of crystal 48 to be constituted by individual mesas 50 arranged in rows and columns so that the face of each such mesa has a rectangular shape. Each mesa 50 contains a p-n junction region 47 and thus each mesa forms a separately functioning LED.

By contrast, the present invention provides a optoelectronic semiconductor chip having a single LED. The single LED of the present invention has recesses forming a plurality of mesas to improve the light output of the LED. The present invention does not relate to individual separately addressable LEDs disposed in an array, as taught by Bailey et al. Bailey seeks to optically isolate the LEDs from one another, whereas the present invention, in the preferred embodiments, permits photons of one mesa region to reach a neighboring mesa for reflection out of the device.

In the present invention, the recesses are formed between the epitaxial active layer and the supporting substrate. The supporting substrate of the present invention provides support for the active layer. The present invention provides cavities within the chip, not at the chip surface as in Bailey. The Bailey structure does not have a supporting substrate but only an LSI memory circuit connected to activate the individual LEDs. The memory circuit is a separate chip from the LED chip of Bailey.

The Bailey reference therefore does not anticipate the invention as claimed.

35 U.S.C. §103(a)

The Bailey reference is discussed above.

The UK reference discloses only an LED with tapered sides, and does not show an LED having recesses to form mesas in the LED.

Even in combination, the two references would not suggest the invention, since no reference teaches or suggest that a single LED have multiple mesas.

The present invention is thus non-obvious over the cited art, whether considered alone or in combination.

Conclusion

Each issue raised in the action has been addressed. Early favorable reconsideration and allowance is hereby requested.

Respectfully submitted,

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